REMARKS

Claims 1-8 are pending in the present application. Claim 5 is amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The applicant notes, with appreciation, that the Office Action indicates at page 2, paragraph 1, that claims 1-4 are allowed.

The specification is objected to for failing to state the meaning of the acronym "HPRIF". The term "HPRIF" is a product-specific term for a register that is included in a product offered by the assignee of the present patent application. An example product including such a register is the S3C2501X 32 Bit RISC Microprocessor product. Pages 4-4 through 4-6 of the User's Manual for the S3C2501X product, including section 4.6 of the manual, are attached hereto as Appendix A. The User's Manual for the S3C2501X product is available at:

http://www.samsung.com/Products/ Semiconductor/SystemLSI/Networks/ PersonalNTASSP/CommunicationProcessor/S3C2501X/um_s3c2501x.pdf.

At the first paragraph of page 4-6 of the User's Manual, the term "HPRIF" refers to the HPRIF Programmable Priority Register for the AHB bus of the product, and the HPRIF term is parenthetically defined as "Programmable Priority Register for Fixed". Accordingly, the HPRIF register is a "programmable priority register". Support for this in the specification as filed can be found at least at the second sentence of the paragraph at page 2, lines 11-14 (i.e., the paragraph amended above) which states that the "priorities of the master blocks can be programmed into the HPRIF register" (emphasis added). This statement is supportive of the HPRIF register being a

"programmable priority register". Accordingly, entry of the amendment and removal of the objection to the specification are respectfully requested.

Independent claim 5 is amended above to state that the arbiter reorders "requested priorities of the bus master corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode". Claim 5 is further amended to state that the arbiter further outputs a "bus master grant signal to the bus master in response to the bus master-selecting signal according to priorities, the bus master grant signal being output from a single, common grant-reordering unit used for operation in both the fixed priority mode and the round-robin mode". These amendments are made in view of comment 2 at page 2 of the Office Action, where the reasons for allowance of independent claim 1 are stated. In view of the above, it is believed that the same reasons for allowance should be extended to apply to amended claim 5. Such allowance is respectfully requested.

Claims 5-8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sato, *et al.* (U.S. Patent Number 5,583,999) in view of "C++ Primer" by Stanley Lippman. Claims 5-8 are further rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Sato, *et al.* Reconsideration of the rejection and allowance of claims 1-8 are respectfully requested.

In the present invention as claimed in independent claim 5, a bus control method includes an arbiter reordering requested priorities of the bus master corresponding to the reordered priority

information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode. The method further includes the arbiter outputting a bus master-selecting signal according to priorities in response to the request-reordering signal, and the arbiter outputting a bus master grant signal to the bus master in response to the bus master-selecting signal according to priorities, the bus master grant signal being output from a single, common grant-reordering unit used for operation in both the fixed priority mode and the round-robin mode.

It is stated in the Office Action, at page 4, lines 4-6, that Sato, *et al.* discloses that priority determining units 11-1, 11-2 prioritize bus masters, and that such function is equivalent to the claimed request-reordering unit. When both a linear method and a round-robin method are used in Sato, *et al.*, the priority determining unit 11-1 is used for the linear method and 11-2 is used for the round-robin method. Therefore, Sato, *et al.* fails to teach or suggest a bus control method that includes an arbiter "reordering requested priorities of the bus masters corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode", as claimed in claim 5.

"C++ Primer" by Stanley Lippman discloses that a pointer variable holds values that are the addresses of objects in memory, and that through a pointer, an object can be referenced indirectly. "C++ Primer" by Stanley Lippman, like Sato, *et al.*, fails to teach or suggest a bus control method that includes an arbiter "reordering requested priorities of the bus masters

corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode", as claimed in claim 5.

Neither Sato, *et al.* nor "C++ Primer" by Stanley Lippman teaches or suggests a bus control method that includes an arbiter "reordering requested priorities of the bus masters corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode", as claimed in claim 5. Accordingly, it is submitted that the combination of Sato, *et al.* and "C++ Primer" by Stanley Lippman fails to teach or suggest the invention as claimed in claim 5. Reconsideration of the rejection of, and allowance of, claim 5 under 35 U.S.C. 103(a) as being unpatentable over Sato, *et al.* and "C++ Primer" by Stanley Lippman are respectfully requested. With regard to the dependent claims 6-8, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of claims 5-8 as being unpatentable over the AAPA in view of Sato, *et al.*, the AAPA discloses the use of separate request-reordering and request-rotating logic units 110, 160 for the fixed priority mode and the round-robin mode, which leads to the limitations described in the specification as filed at page 4, line 20 through page 5, line 12.

The AAPA fails to teach or suggest a bus control method that includes an arbiter "reordering requested priorities of the bus masters corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering

unit used for operation in both the fixed priority mode and the round-robin mode", as claimed in claim 5. Instead, in the AAPA, separate request-reordering and request-rotating logic units 110 and 160 are used for the fixed priority mode and the round-robin mode, respectively.

Neither the AAPA nor Sato, *et al.*, as discussed above, teaches or suggests a bus control method that includes an arbiter "reordering requested priorities of the bus masters corresponding to the reordered priority information and outputting a request-reordering signal at a single, common request-reordering unit used for operation in both the fixed priority mode and the round-robin mode", as claimed in claim 5. Accordingly, it is submitted that the combination of the AAPA and Sato, *et al.* fails to teach or suggest the invention as claimed in claim 5. Reconsideration of the rejection of, and allowance of, claim 5 under 35 U.S.C. 103(a) as being unpatentable over the AAPA and Sato, *et al.* are respectfully requested. With regard to the dependent claims 6-8, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: March 20, 2006

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S3C2501X

32-BIT RISC MICROPROCESSOR USER'S MANUAL

Revision 1

SAMSUNG ELECTRONICS

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S3C2501X RISC Microprocessor
User's Manual, Revision 1
Publication Number: 21-S3-C2501X-122002

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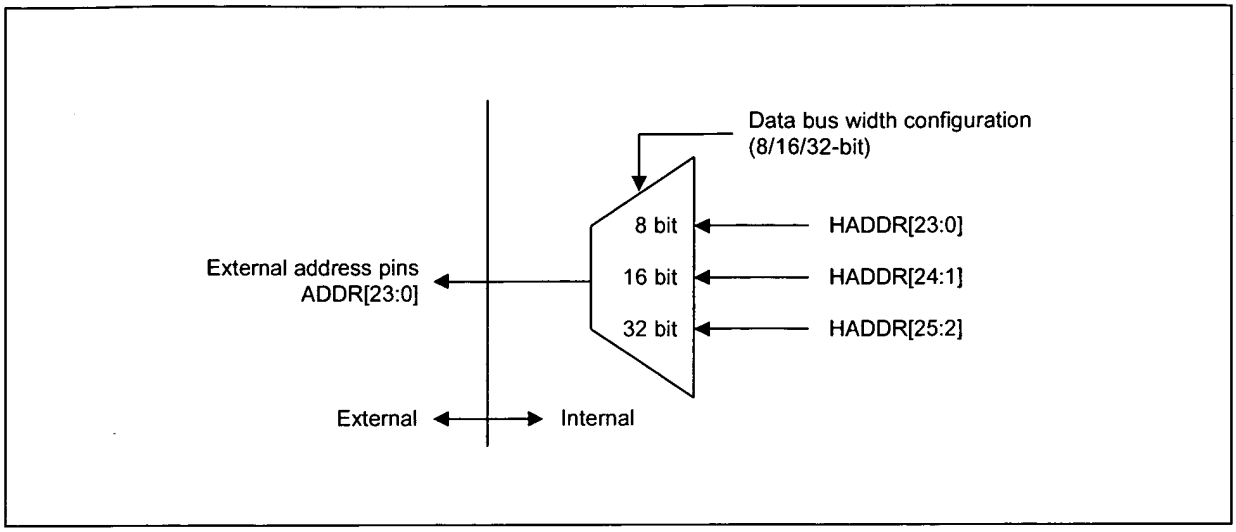


Figure 4-2. External Address Bus Diagram

4.6 ARBITRATION SCHEME

The S3C2501X can support the fixed priority and the round-robin method for AHB bus arbitration by register setting. Especially, the S3C2501X can program the priority order in the fixed priority mode as well as the ratio of the bus occupancy in the round-robin priority mode.

The internal function blocks or AHB bus masters are divided into three groups, Group A, Group B, and Group C. Group A has only Test Interface Controller (TIC) block. The Group A has the highest bus priority. Group B has 3 AHB bus masters, General DMA, Ethernet Controller 0, Ethernet Controller 1. The S3C2501X can program the bus priority of each bus masters among Group B. So the bus priority of bus masters in only Group B can be programmed. Group C has the ARM940T CPU. The relative priority of Group B and Group C is determined more or less in an alternating manner.

The local priority of six channels of general DMA can be programmed by fixed priority or round-robin priority in similar manner to the AHB bus priority. Please refer to the general DMA chapter.

Table 4-2. AHB Bus Priorities for Arbitration

Function Block	AHB Bus Priority (Group)
Test Interface Controller (TIC)	Group A (highest priority)
General DMA (GDMA)	Group B
Ethernet Controller 0	Group B
Ethernet Controller 1	Group B
ARM940T CPU	Group C

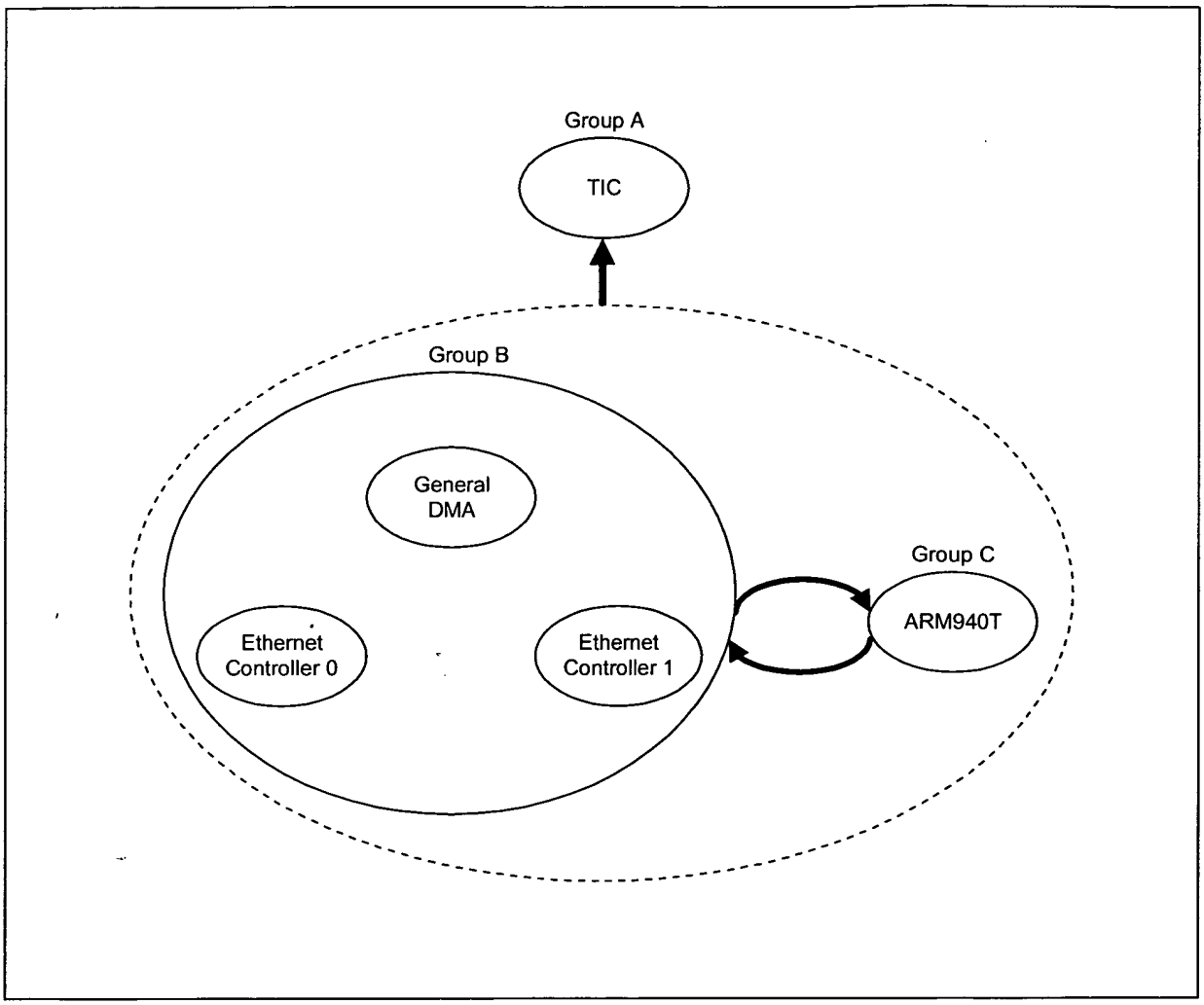


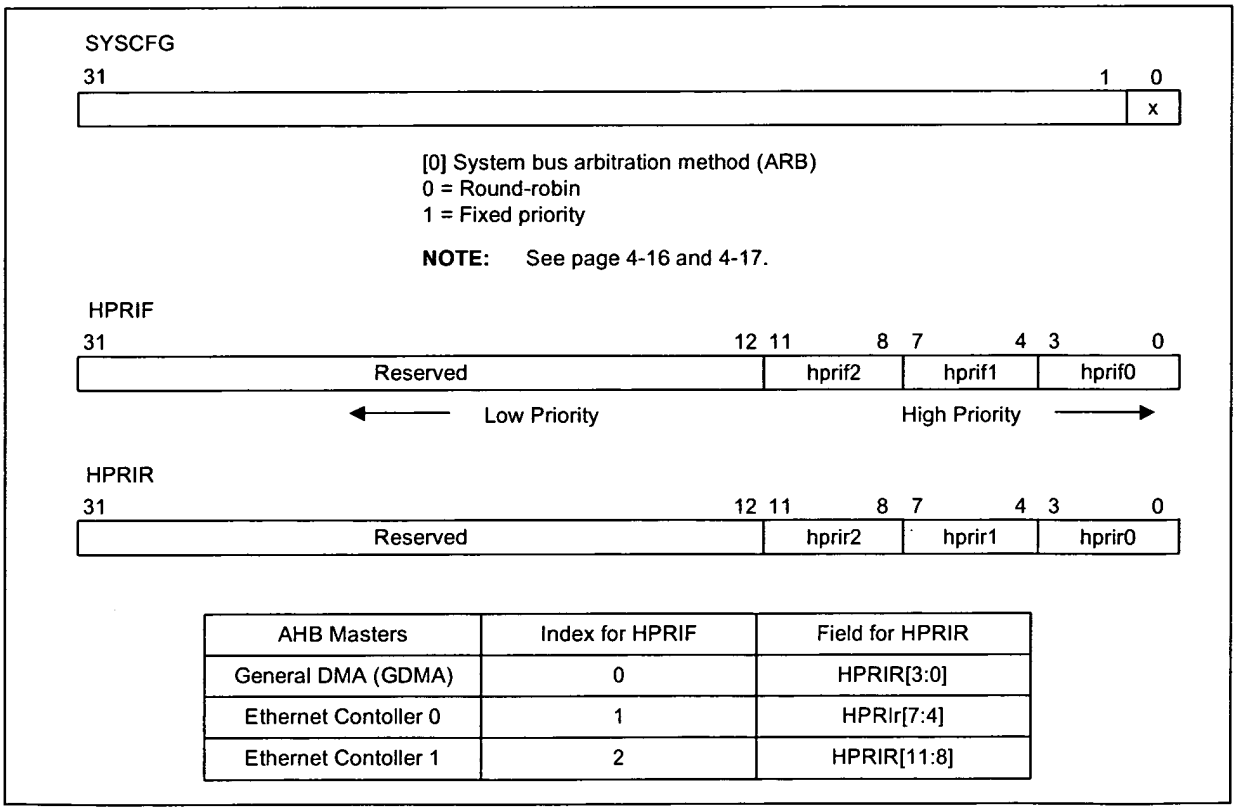
Figure 4-3. Priority Groups of S3C2501X

AHB Bus Programmable Priority Registers are HPRIF(Programmable Priority Register for Fixed) and HPRIR (Programmable Priority Register for Round-Robin).

If system configuration register (0xF0000000) SYSCFG[0] = 0x1, the programmable fixed priority is run by HPRIF register. Each master has its own fixed priority index. For example, GDMA has the index 0. The index for each master is shown in Figure 4-4. The reset value of HPRIF register is 0x00543210. The first field of HPRIF[3:0] indicates the highest priority and the HPRIF[7:4] indicates the second highest priority and so on. HPRIF[23:12] should not be writtern any value and must always be 0x543.

The users are allowed to program HPRIF[11:0]. When the SYSCFG[0] = 0x1 and the HPRIF is 0x00543012, the fixed priority order form the highest to the lowest is Ethernet controller1, ethernet controller0 and General DMA.

If system configuration register (0xF0000000) SYSCFG[0] = 0x0, the programmable round-robin priority is run by HPRIR register. All AHB bus masters own their respective field position in HPRIR. The ratio of the bus occupancy can be programmed by writing an arbitrary value on each field. The arbitrary value can be 0x0 to 0xF.
The reset value of HPRIR register is 0x00000000. The position for each master is shown in Figure 4-4.
The ratio of the bus occupancy of the bus master in the first field is intended to be (hprir0+1)/((hprir2+1)+(hprir1+1)+(hprir0+1)+3) and so on. However, the arbiter of S3C2501X has a fairness problem.
The HPRIR should be programmed by the value of 0x000330 to have the same occupancy ratio for three masters.
The arbiter has a problem that the GDMA always has three more chances to occupy the bus than other masters. Therefore, hprir2 and hprir1 should have the value of (hprir0+3) to keep the same occupancy ratio.



AHB Masters	Index for HPRIF	Field for HPRIR
General DMA (GDMA)	0	HPRIR[3:0]
Ethernet Contoller 0	1	HPRIr[7:4]
Ethernet Contoller 1	2	HPRIR[11:8]

Figure 4-4. AHB Programmable Priority Registers